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⑤発明の名称　半導体装置の製造方法

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明　細　書

1、発明の名称

半導体装置の製造方法

2、特許請求の範囲

(1) 表面の少なくとも一部分に、その法線が基板主面法線と80°以上の角度をなす傾斜部を有する半導体基板上に第1の絶縁膜を形成する第1の工程と、前記第1の絶縁膜の一部をエッチングし、前記傾斜部における絶縁膜表面の法線が基板主面法線と60°～85°の角度をなす様に加工する第2の工程と、前記第1の絶縁膜上に気相反応により第2の絶縁膜を形成する第3の工程を備えてなることを特徴とする半導体装置の製造方法。

(2) 第2の工程が第1の絶縁膜をアルゴンガスおよび弗化物ガスを含むプラズマ中でエッチングすることを特徴とする特許請求の範囲第1項記載の半導体装置の製造方法。

(3) 第2の工程が、第1の絶縁膜を、その凹部内にレジストを形成した後に、酸素および弗化物ガスを含むプラズマ中でエッチングすることを特徴とする特許請求の範囲第1項記載の半導体装置の製造方法。

(4) 第2の絶縁膜を形成する第3の工程が有機オキシシランとオゾンの熱分解反応が有機オキシシランと酸素のプラズマ生成によるプラズマ分解反応のうち少なくともどちらかの反応か、または前記2反応のくり返しによって絶縁膜を形成する工程であることを特徴とする特許請求の範囲第1から第3項のいずれかに記載の半導体装置の製造方法。

3、発明の詳細な説明

産業上の利用分野

本発明は超LSIなどの高集積化に際し、多層配線における層間絶縁膜に用いられ、微細な凹凸を有する基板上に絶縁膜を堆積するのに有効な半導体装置の製造方法に関する。

従来の技術

LSIの集積度が増すにつれ、配線を多層に積み重ねる技術が用いられており、微細な配線間に

絶縁膜を埋込むとともに平坦な層間絶縁膜を形成する必要がある。そこで、従来では気相成長法（以下ＣＶＤ法と記す）により、微細な配線間へのＳｉＯ$_2$膜等の絶縁膜の堆込みの検討が種々なされている。例えば、第４図に示すように、第４図Ａにおいて、Ｓｉ基板１００にＡｌ配線パターン１０２（１０２Ａ～１０２Ｃ）が形成されている上にテトラエトキシシラン（ＴＥＯＳ）のような有機オキシシラン類を原料ガスとしてプラズマＣＶＤ法で酸素と反応させＳｉＯ$_2$膜１０４を堆積する。上記例に示したように、有機オキシシランを用いたＳｉＯ$_2$膜はシラン系ガスの反応によるＳｉＯ$_2$膜に比べオーバーハングが少なく、良好な段差被覆性を有しているので、配線間隙を埋込むのに適している。（例えばＶＬＳＩマルチレベル　インターコネクション　コンファレンス（ＩＥＥＥ　ＶＭＩＣ）June15-16,1987 M.J.Thoa "A1.0μmCMOS　LEVEL METAL TECHNOLOGY INCORPORATING PLASMA ENHANCED TEOS" 参照）

特徴を有しているが、平坦部膜厚が凹部内の膜厚に比べ２倍程度厚いため、間隙のアスペクト比が０．８以上になると、第４図Ｂに示すように空隙１０８（１０８Ａ～１０８Ｂ）が生じてしまう。また、第５図に示すように、Ａｒスパッタ法によりＳｉＯ$_2$膜１０４の角を４５°の角度でエッチングする例においても、Ａｌ配線間隙のアスペクト比が１以上になると、素子特性の劣化を防止するためＡｌ配線１０２（１０２Ａ～１０２Ｃ）表面を直接Ａｒスパッタしないようにした場合、間隙底部まで傾斜を有するようにＳｉＯ$_2$膜１０４をエッチングすることができない。そのためＳｉＯ$_2$膜１０６を堆積した際、第５図Ｃに示すように空隙１０８（１０８Ａ～１０８Ｂ）が生じてしまう。

本発明は、このような従来の問題に鑑み、これらの問題点を解決し、製造歩留り及び信頼性に優れ、高集積化を可能とする半導体装置の製造方法を提供することを目的とする。

課題を解決するための手段

また、その他の例では、第５図に示すように、Ｓｉ基板１００にＡｌ配線パターン１０２（１０２Ａ～１０２Ｃ）が形成されている上にＴＥＯＳとO_2のプラズマ反応によりＳｉＯ$_2$膜１０４を堆積した後、Ａｒスパッタ法によりＳｉＯ$_2$膜１０４の角を４５°の角度でエッチングしＳｉＯ$_2$膜１０５を得る。そして、再びＴＥＯＳとO_2のプラズマ反応によりＳｉＯ$_2$膜１０６を堆積して層間絶縁膜を形成する。このように、ＡｒスパッタによりＳｉＯ$_2$膜の角を４５°の角度でエッチングすることによって、より微細な間隙を埋め込むことができる（電子材料1987年9月P.116-P.122「PRECISION5000ＣＶＤとその機能」参照）。

発明が解決しようとする課題

しかし、第４図及び第５図に示す従来の製造方法においては、下記のような問題点がある。

微細な、特にアスペクト比が１以上の配線間隙を埋込むことができない。つまり第４図に示す例では、ＴＥＯＳを原料としたプラズマＣＶＤ法によるＳｉＯ$_2$膜はオーバーハングが少ないという

本発明は、表面の少なくとも一部分に、その法線が基板主面法線と８０°以上の角度をなる傾斜部を有する半導体基板上に第１の絶縁膜を形成する第１の工程と、前記第１の絶縁膜の一部をエッチングし、前記傾斜部における絶縁膜表面の法線が基板主面法線と６０°～８５°の角度をなす様に加工する第２の工程と、前記第１の絶縁膜上に気相反応により第２の絶縁膜を形成する第３の工程を備えてなることを特徴とする半導体装置の製造方法である。

作　用

本発明は上記構成により、次のように作用する。

(1) 傾斜部における第１の絶縁膜表面の法線が基板主面法線と６０°～８５°の角度をなす様に第１の絶縁膜を加工することにより、第２の絶縁膜を形成した際、アスペクト比が１以上の間隙を空隙なく埋込むことができる。

(2) 空隙を生じることなく微細な間隙を埋めこむことができるので、半導体基板表面の平坦化工程

が容易となり、上層の配線の形成が容易になる。また、下層の配線の断線が防止できる。

(2) 有機オキシシランの熱分解反応による絶縁膜の形成工程とプラズマ分解反応による絶縁膜の形成工程を組合わせることによって、微細な凹部への絶縁膜の埋込みを容易にできる。

実施例

実施例1

以下、本発明の製造方法を具体例に基づいて説明する。

第1図A～Cは本発明による一実施例の製造工程で2層配線の層間絶縁膜形成工程を示す。第1図Aに示す半導体Si基板2に回路素子が形成され、基板主面に対してほぼ垂直な側面を有する第1のAl配線4A～4C(全体を言うときはAl配線4と記す)が形成された基板をプラズマCVD装置内に設置し、基板温度を390℃に保ち、TEOSとO_2の混合ガスを導入し、真空度が1.0Torrの状態でプラズマを生成し、第1の絶縁膜としてのSiO_2膜6を0.6μm堆積する。しかる後に、第1図Bに示すように、上記Aで示す基板をドライエッチング装置内に設置し、CF_4とArの混合ガスを導入し、真空度が0.05Torrの状態でプラズマ生成し、SiO_2膜6を0.3μmエッチングして、SiO_2膜8を得る。このとき、ArガスによりSiO_2膜6を45°の角度でエッチングしながら、CF_4ガスによりSiO_2膜6を異方性エッチングすることによって、Al配線(4A～4C)の間隙内のSiO_2膜8が間隙底部まで60°～85°の角度の傾斜をもつ様に加工することができる。この後、第1図Cに示すように、上記Bで示す基板をプラズマCVD装置内に設置し、基板温度を390℃に保ち、TEOSとO_2の混合ガスを導入し、真空度が1.0Torrの状態でプラズマ生成し、第2の絶縁膜としてのSiO_2膜10を0.5μm堆積する。このとき、SiO_2膜8は間隙底部まで60°～85°の傾斜を有し、基板主面に対し垂直かあるいはそれ以上の角度を有する側面を持たないので、SiO_2膜10によりアスペクト比が1以上のAl配線4(4A～4C)の間隙を空隙なく埋込むことができる。

なお、上記第1の絶縁膜を形成するプラズマCVDにおいて、TEOSとO_2の代りにSiH_4とO_2あるいはSiH_4とN_2Oを用いても同様の結果が得られる。また、上記ドライエッチングにおいて、CF_4の代りにCHF_3を用いても同様の結果が得られる。また、上記第1及び第2の絶縁膜を形成するプラズマCVDにおいて、TEOSの代りにテトラメトキシシラン($Si(OCH_3)_4$)を用いても同様の結果が得られる。

また、述べるまでもなく上記SiO_2膜6をエッチングしてSiO_2膜8を得る工程において、Al配線4間隙内のSiO_2膜8の基板主面に対する傾斜が85°に近いほど、より微細なAl配線間隙を空隙なく埋込むことができる。また、このエッチング工程において、Al配線4(4A～4C)表面を直接Arプラズマ雰囲気中にさらすことなく、間隙底部までSiO_2膜8に傾斜を形成することができるので、回路素子にArプラズマによる損傷を与えることがない。

また、上記実施例は、基板主面に対してほぼ垂直な側面を有するAl配線上に層間絶縁膜を形成する場合について述べたが、上記実施例の製造方法はAl配線が基板主面に対して90°以上の角度の側面を有する場合においても、同様の効果を得ることができる。

実施例2

第1図を用いて、本発明による第2の製造工程実施例の2層配線の層間絶縁膜形成工程を示す。第1図AでSi基板2に回路素子が形成され、基板主面に対してほぼ垂直な側面を有する。

第1のAl配線4(4A～4C)が形成された基板に実施例1と同様にプラズマCVD法を用いて、第1の絶縁膜としてのSiO_2膜6を0.6μm堆積する。そして、第1図Bに示すように、実施例1と同様にArおよび赤化物ガスを用いたドライエッチング法によって、SiO_2膜6を0.3μmエッチングとして60°～85°の傾斜を有するSiO_2膜8を得る。しかる後に、第1図C

に示すように、基板を熱CVD装置内に設置し、基板温度を390℃に保ち、TEOSとO_3の混合ガスを導入し、真空度が60Torrの状態で熱反応により第2の絶　膜としてのSiO_2膜10を0.5μm堆積し、Al配線4の間隔を埋込む。

なお、上記第2の絶縁膜を形成する熱CVDにおいて、TEOSの代わりにテトラメトキシシラン（$Si(OCH_3)_4$）を用いても同様の結果が得られる。

実施例3

第2図を用いて本発明による第3の実施例の製造工程で2層配線の層間絶縁膜形成工程を示す。第2図AでSi基板2に回路素子が形成され、基板主面に対してほぼ垂直な側面を有する第1のAl配線4（4A～4C）が形成された基板に実施例1と同様にプラズマCVD法を用いて、第1の絶縁膜としてのSiO_2膜6を0.6μm堆積する。しかる後に第2図Bに示すように、基板上にレジスト膜7を1.5μm程度の厚さで塗布し、基板表面を平坦化する。その後、基板をドライエッチング装置内に設置し、O_2ガスを導入し、真空度が0.1 Torrの状態でプラズマ生成し、前記レジスト膜7を1.5μmエッチングし、第2図Cに示すようにSiO_2膜6上の凹部にレジスト膜7（7A～7D）を形成する。しかる後に、第2図Dに示すように、基板をドライエッチング装置内に設置し、C_2F_6とO_2の混合ガスを導入し、真空度が2Torrの状態でプラズマ生成し、前記レジスト膜7（7A～7D）及びSiO_2膜6をエッチングして、SiO_2膜8を得る。このとき、O_2ガスによりレジスト膜7（7A～7D）をエッチングしながら、C_2F_6とO_2の混合ガスによりSiO_2膜6を等方性エッチングすることによって、Al配線4（4A～4C）の間隔内のSiO_2膜8を間隔底部まで60°～85°の角度の傾斜をもつ様に加工することができる。このとき、SiO_2膜8には基板主面に対して垂直な側面は残存しない。この後第2図Eのように、実施例1と同様にプラズマCVD法を用いて、第2の絶縁膜としてのSiO_2膜10を0.5μm堆積し、Al配線4の間隔を埋込む。

なお、上記実施例3において、TEOSとO_3を用いたプラズマCVD法により第2の絶縁膜を形成する代わりに、実施例2のごとくTEOSとO_3を用いた熱CVD法により第2の絶縁膜を形成しても同様の結果が得られる。

実施例4

第3図を用いて本発明による第4の実施例の製造工程で2層配線の層間絶縁膜の形成工程を示す。第3図AでSi基板2に回路素子が作成され、基板主面に対してほぼ垂直な側面を有する第1のAl配線4（4A～4C）が形成された基板に実施例1と同様にプラズマCVD法を用いて、第1の絶縁膜としてのSiO_2膜6を0.6μm堆積する。しかる後に第3図Bに示すように、実施例1と同様にArおよび弗化物ガスを用いたドライエッチング法によって、SiO_2膜6を0.3μmエッチングして60°～85°の傾斜を有するSiO_2膜8を得る。次に、第3図Cに示すように、実施例2と同様にTEOSとO_3の混合ガスによる熱CVD法でSiO_2膜9を0.2μm堆積し、前記Al配線4の0.8μm以下の間隔を埋込む。そして、第3図Dに示すように、実施例1と同様にTEOSとO_2の混合ガスによるプラズマCVD法でSiO_2膜10を0.3μm堆積する。このとき、TEOSの熱反応によるSiO_2膜9はTEOSのプラズマ反応によるSiO_2膜10よりも段差被覆性が優れており、1μm以下の間隔を埋込むのに適している。しかし、このTEOSの熱反応によるSiO_2膜9は膜質が悪く、厚く堆積すると後の熱処理の工程においてクラックが生じる恐れがあり、TEOSのプラズマ反応によるSiO_2膜10を堆積することによって、クラックの発生を防止することができる。また、TEOSの熱反応によるSiO_2膜の堆積速度が0.2μm／minであるのに比べ、TEOSのプラズマ反応によるSiO_2膜の堆積速度は0.8μm／minと速いので、スループットの向上が図れる。また、上記TEOSの熱反応によるSiO

$_2$膜厚と上記ＴＥＯＳのプラズマ反応によるSiO_2膜厚を適当に選び、これら各工程をくり返すことによって、任意の寸法の前記Ａ１配線４の間隙を埋込むことができる。

なお、上記実施例４において、Ａｒおよび弗化物ガスを用いたドライエッチング法により、６０°～８５°の傾斜を有するようにSiO_2膜６をエッチングする代りに、実施例３のごとく、SiO_2膜６の上の回部にレジスト膜を形成した後、O_2および弗化物ガスを用いたドライエッチング法によりSiO_2膜６をエッチングしても同様の結果が得られる。

発明の効果

以上述べてきたように本発明の半導体装置の製造方法によれば、次のような効果が得られる。

間隙に形成した第１の絶縁膜を間隙底部まで６０°～８５°の傾斜を有し、基板主面に対し垂直な側面が残らないようにエッチングすることにより、第２の絶縁膜を形成した際、アスペクト比が１以上の微細な間隙を空隙なく埋込むことができる。

空隙を生じることなく微細な間隙を埋込むことができるので、半導体基板表面の平坦化工程が容易となり、多層配線の層間絶縁膜の形成に適用すれば、上層の配線の形式が用意になる。また、下層の配線の断線が防止できる。さらには、多層配線を実現することにより、素子の高集積化ならびに高速化が図れる。

有機オキシシランの熱分解反応による絶縁膜の堆積工程とプラズマ分解反応による絶縁膜の堆積工程を組合わせることによって、微細な回部への絶縁膜の埋込みを容易にできる。

以上のように、本発明は微細な回部に空隙を生じることなく絶縁膜を埋込むことができるため、素子の高集積化ならびに信頼性の向上に大きく寄与するものである。

４．図面の簡単な説明

第１図は本発明による半導体装置の製造方法の実施例１及び２を説明するための工程断面図、第２図は本発明による製造方法の実施例３を説明するための工程断面図、第３図は本発明による製造方法の実施例４を説明するための工程断面図、第４図は従来の製造方法の一実施例を説明するための工程断面図、第５図は従来の製造方法の他の実施例を説明するための工程断面図である。

２……Ｓｉ基板、４Ａ，４Ｂ，４Ｃ，……Ａｌ配線、６，８，９，１０……ＣＶＤ－SiO_2膜、７，７Ａ，７Ｂ，７Ｃ，７Ｄ……レジスト膜。

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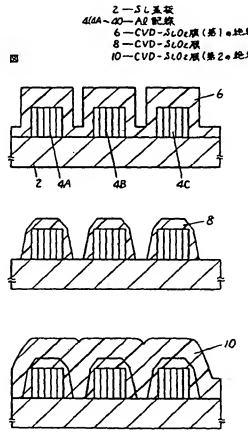
第１図

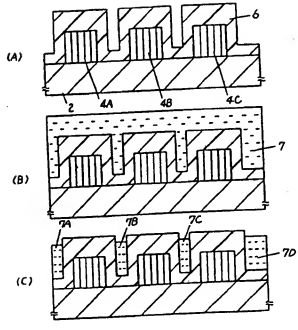


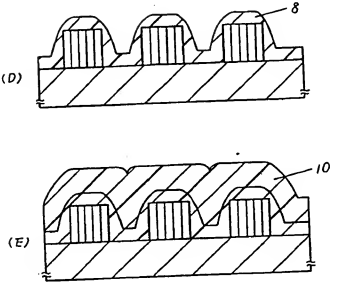
7, 7A, 7B, 7C — レジスト膜

8 — CVD-SiO2膜

第 2 図

第 2 図

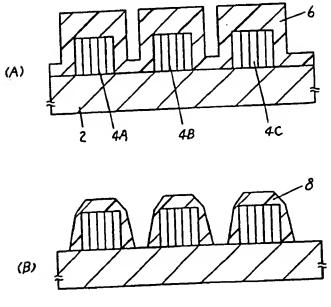


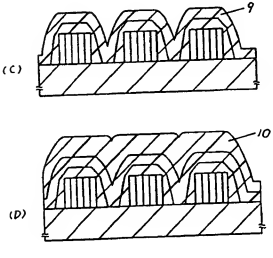


9, 10 — CVD-SiO2膜 (第2の絶縁膜)

第 3 図

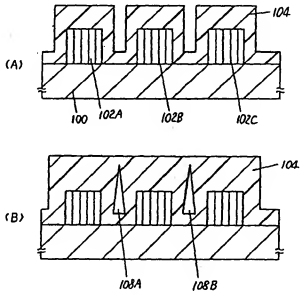
第 3 図





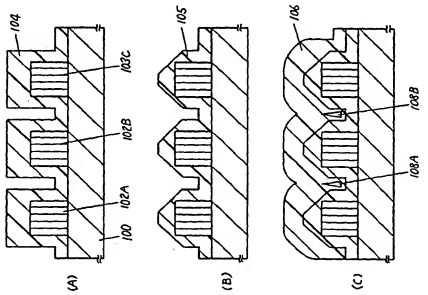
100 — Si基板
102(102A～102C) — Al配線
104 — CVD－SiO₂膜
108(108A・108B) — 空隙

第 4 図



105, 106 — CVD－SiO₂膜

第 5 図



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METHOD FOR MANUFACTURING SEMICONDUCTOR DEVICE

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[There are no amendments to this patent.]

Claims

1. A method for manufacturing a semiconductor device characterized by the fact that it has the following steps of operation: a first step in which a first insulating film is formed on a semiconductor substrate that has at least a portion of its surface formed as a slope portion with its normal forming an angle of 80° or larger with respect to the normal to the principal surface of the substrate; a second step in which a portion of said first insulating film is etched so that the normal to the surface of the insulating film on said slope portion forms an angle of 60-85° with respect to the normal to the principal surface of the substrate after this step of processing; and a third step in which a second insulating film is formed on said first insulating film by means of chemical vapor deposition.

2. The method for manufacturing a semiconductor device described in Claim 1 characterized by the fact that in the second step, the first insulating film is etched in a plasma containing argon gas and a fluorine containing gas.

3. The method for manufacturing a semiconductor device described in Claim 1 characterized by the fact that in the second step, the first insulating film is etched in a plasma containing oxygen and a fluorine containing gas after formation of a resist in its recessed portions.

4. The method for manufacturing a semiconductor device described in any of Claims 1-3 characterized by the fact that the third step, in which the second insulating film is formed, is a step in which the insulating film is formed by means of either a pyrolysis reaction of organic oxysilane and ozone or a plasma decomposition reaction of organic oxysilane and oxygen by means of plasma generation, or by repeatedly performing said two reactions.

Detailed explanation of the invention

Industrial application field

This invention pertains to a method for manufacturing a semiconductor device. The method of this invention can be effectively used in depositing an insulating film on a substrate

having fine bumps and dips. Said insulating film can be used as an interlayer insulating film in a multi-layer wiring for increasing the integration degree of a super-LSI, etc.

Prior art

With increase in the integration degree of LSIS, technology for depositing wiring as a multi-layer structure has been used. It is thus necessary to cover portions between fine wiring portions with an insulating film and to form a flat interlayer insulating film. In the prior art, extensive studies have been conducted on using a chemical vapor deposition method (hereinafter referred to as CVD method) to cover an SiO_2 film or another insulating film between fine wiring portions. For example, Figure 4 illustrates such a process. As shown in Figure 4A, on Si substrate (100), on which Al wiring pattern (102) (102A-102C) is formed, SiO_2 film (104) is deposited by means of a reaction between tetraethoxysilane (TEOS) or other organic oxysilanes as a feed gas with oxygen by means of a plasma CVD method. Compared with an SiO_2 film prepared in a reaction of a silane based gas, the SiO_2 film prepared using an organic oxysilane as shown in the aforementioned example has less overhang, and the step covering property is good. Consequently, it is appropriate for covering up the gaps between wiring portions. (For example, see: VLSI Multi-Level Interconnection Conference (IEEE VMIC) June 15-16, 1987 M.J. Thoma "A 1.0 μm CMOS LEVEL METAL TECHNOLOGY INCORPORATING PLASMA ENHANCED TEOS.")

Figure 5 illustrates another example. In this example, on Si substrate (100) with Al wiring pattern (102) (102A-102C) formed on it, SiO_2 film (104) is deposited by means of a plasma reaction between TEOS and O_2. Then, using an Ar sputtering method, SiO_2 film (104) is etched at an angle of 45° to form SiO_2 film (105). Then, by means of a plasma reaction of TEOS and O_2, SiO_2 film (106) is deposited again to form an interlayer insulating film. In this way, by means of etching of the SiO_2 film at an angle of 45° by means of Ar sputtering, it is possible to cover up even finer gaps (Denshi Zairyo, September 1987, pp. 116-122 "Precision 5000 CVD and its functions").

Problems to be solved by the invention

However, the conventional manufacturing methods shown in Figures 4 and 5 have the following problems.

It is impossible to cover up fine wiring gaps, especially those with an aspect ratio of 1 or larger. That is, in the example illustrated in Figure 4, although the SiO_2 film prepared using a plasma CVD method with TEOS as a feed material has a characteristic feature that its overhang is small, the thickness of the film of the flat portion is nevertheless about twice that of the film pressure [sic; thickness] inside the recessed portion. Consequently, with an aspect ratio of the

gap of 0.8 or larger, voids (108) (108A-108B) are formed as shown in Figure 4B. Also, in the example shown in Figure 5, in which an SiO_2 film (104) is etched at an angle of 45° by means of an Ar sputtering method, when the aspect ratio of the Al wiring gap becomes 1 or larger, and Ar sputtering is not performed directly on Al wiring (102) (102A-102C) so as to prevent degradation in the element characteristics, it is impossible to etch SiO_2 film (104) with a slope reaching the bottom of the gap. Consequently, when SiO_2 film (106) is deposited, voids (108) (108A-108B) are formed as shown in Figure 5C.

The objective of this invention is to solve the aforementioned problems of the conventional methods by providing a method for manufacturing a semiconductor device characterized by the fact that it has excellent manufacturing yield and reliability and allows a high integration degree.

Means to solve the problems

This invention provides a method for manufacturing a semiconductor device characterized by the fact that it has the following steps of operation: a first step in which a first insulating film is formed on a semiconductor substrate that has at least a portion of its surface formed as a slope portion with its normal forming an angle of 80° or larger with respect to the normal to the principal surface of the substrate; a second step in which a portion of said first insulating film is etched so that the normal to the surface of the insulating film on said slope portion forms an angle of 60-85° with respect to the normal to the principal surface of the substrate after this step of processing; and a third step in which a second insulating film is formed on said first insulating film by means of chemical vapor deposition.

Operation of the invention

This invention with the aforementioned constitution has the following operation.

(1) Since the first insulating film is processed so that the normal to the surface of the first insulating film in the slope portion forms an angle of 60-85° with respect to the normal to the principal surface of the substrate, when the second insulating film is formed, it is possible to cover up gaps with an aspect ratio of 1 or larger free of voids.

(2) Because it is possible to cover up fine gaps free of voids, it is easy to perform the flattening operation for the surface of the semiconductor substrate, and it is easy to form the upper layer of wiring. Also, it is possible to prevent wire breakage of the lower layer.

(3) By means of a combination of the step of formation of insulating film by means of pyrolysis of organic oxysilane and the step of formation of an insulating film by means of plasma decomposition reaction, it is easy to cover the insulating film in fine recessed portions.

Application examples

Application Example 1

In the following, this invention will be explained in detail with reference to application examples.

Figures 1A-C illustrate steps of operation for forming an interlayer insulating film of two layers of wiring in a manufacturing process of an application example of this invention. As shown in Figure 1A, circuit elements were formed on semiconductor Si substrate (2), and the substrate having first Al wirings (4A)-(4C) (as a whole, they will be referred to as Al wiring (4)) with side surfaces almost perpendicular to the principal surface of the substrate was set in a plasma CVD apparatus. While the temperature of the substrate was kept at 390°C, a gas mixture of TEOS and O_2 was fed in, and a plasma was generated while a vacuum was maintained at 10 torr. In this way, as the first insulating film, SiO_2 film (6) with a thickness of 0.6 μm was deposited. Then, as shown in Figure 1B, the substrate illustrated in said [Figure 1] A was set in a dry etching apparatus. Then, a gas mixture of CF_4 and Ar was fed in, and a plasma was generated while a vacuum was maintained at 0.05 torr. In this state, SiO_2 film (6) was etched for 0.3 μm, forming SiO_2 film (8). In this case, while SiO_2 film (6) was etched at an angle of 45° with Ar gas, SiO_2 film (6) was conventionally anisotropically etched with CF_4 gas, so that SiO_2 film (8) inside the gaps of Al wiring (4A-4C) could be processed with a slope angle of 60-85° down to the bottom of the gaps. Then, as shown in Figure 1C, the substrate shown in said [Figure 1] B was set in a plasma CVD apparatus. While the substrate temperature was kept at 390°C, a gas mixture of TEOS and O_2 was fed in, and a plasma was generated while a vacuum was maintained at 10 torr. In this way, as a second insulating film, SiO_2 film (10) with a thickness of 0.5 μm was deposited. In this case, because SiO_2 film (8) has a slope with angle in the range of 60-85° down to the bottom of the gap, and none of its side surface is perpendicular to the principal surface of the substrate or has an even larger angle, it is possible for SiO_2 film (10) to cover up the gaps of Al wiring (4) (4A-4C) with an aspect ratio of 1 or larger.

Also, the same results were obtained when SiH_4 and O_2 or SiH_4 and N_2O were used in place of TEOS and O_2 in said plasma CVD for forming said first insulating film. Also, the same results were obtained when CHF_3 was used in place of CF_4 in said dry etching. Also, in the plasma CVD for forming said first and second insulating films, the same results were obtained when tetramethoxysilane [$Si(OCH_3)_4$] was used in place of TEOS.

Also, in said process for forming SiO_2 film (8) by etching SiO_2 film (6), it has been found that the nearer the angle of the slope of the SiO_2 film (8) in the gaps of Al wiring (4) with respect to the principal surface of the substrate to 85°, the finer the Al wiring gaps that can be covered up free of voids. Also, in this etching operation, it is possible to form a slope of SiO_2 film (8) down

to the bottom of the gaps without exposing the surface of Al wiring (4) (4A-4C) directly to the Ar plasma atmosphere. Consequently, the circuit elements are not damaged by the Ar plasma.

Also, in the aforementioned application example, we have described an example wherein an interlayer insulating film is formed on Al wiring having side surfaces almost perpendicular to the principal surface of the substrate. However, the manufacturing method of the aforementioned application example can also be used if the side surfaces of the Al wiring have angles of 90°C or larger with respect to the principal surface of the substrate. The same effects as aforementioned can be realized in this case.

Application Example 2

Figure 1 can be used to illustrate the process for forming an interlayer insulating film of a 2-layer wiring in Application Example 2 of the manufacturing operation in this invention. As shown in Figure 1A, circuit elements were formed on Si substrate (2), with side surfaces [of wiring] almost perpendicular to the principal surface of the substrate.

Using the same plasma CVD method as that used in Application Example 1, as a first insulating film, SiO_2 film (6) with a thickness of 0.6 μm was deposited on the substrate where the first Al wiring Al 4 (4A-4C) had been formed. Then, as shown in Figure 1B, the same gas mixture of Ar and fluorine containing gas as that used in Application Example 1 was used in a dry etching method to etch SiO_2 film (6) for 0.3 μm to form SiO [sic; SiO_2] film (8) with a slope of 60-85°. Then, as shown in Figure 1C, the substrate was set in a thermal CVD apparatus. While the substrate temperature was kept at 390°C, a gas mixture of TEOS and O_3 was fed in, and thermal reaction was performed with a vacuum degree of 60 torr to deposit SiO_2 film (10) with a thickness of 0.5 μm as a second insulating film that covered up the gaps of Al wiring (4).

The same results were obtained when tetramethoxysilane [$Si(OCH_3)_4$] was used in place of TEOS in the thermal CVD for forming said second insulating film.

Application Example 3

Figure 2 can be used to illustrate the steps of formation of an interlayer insulating film for a 2-layer wiring in the manufacturing process of Application Example 3 in this invention. As shown in Figure 2A, circuit elements were formed on Si substrate (2), with first Al wiring (4) (4A-4C) having side surfaces almost perpendicular to the principal surface of the substrate. Then, using the same plasma CVD method as that used in Application Example 1, SiO_2 film (6) with a thickness of 0.6 μm was formed as a first insulating film on said substrate. Then, as shown in Figure 2B, resist film (7) with a thickness of 1.5 μm was coated on the substrate to flatten the surface above the substrate. Then, the substrate was set in a dry etching apparatus. O_2 gas was fed in, and a plasma was generated at a vacuum degree of 0.1 torr. As a result, said resist film (7)

was etched for 1.5 μm, and, as shown in Figure 2C, resist film (7) (7A-7D) was formed in recessed portions of SiO_2 film (6). Then, as shown in Figure 2D, the substrate was set in the dry etching apparatus, and a gas mixture of C_2F_6 and O_2 was fed in, and a plasma was generated under a vacuum degree of 2 torr. In this way, said resist film (7) (7A-7D) and SiO_2 film (6) were etched to form SiO_2 film (8). In this case, while resist film (7) (7A-7D) was etched with O_2 gas, SiO_2 film (6) was subject to isotropic etching with the gas mixture of C_2F_6 and O_2. As a result, SiO_2 film (8) inside the gaps of Al wiring (4) (4A-4C) was processed to a slope with an angle of 60-85° down to the bottom of the gaps. In this case, no side surface of SiO_2 film (8) perpendicular to the principal surface of the substrate was left. After that, as shown in Figure 2E, the same plasma CVD method as that used in Application Example 1 was used to deposit SiO_2 film (10) with a thickness of 0.5 μm as a second insulating film to cover up the gaps of Al wiring (4).

Also, the same results were obtained when the second insulating film was formed by means of the thermal CVD method using TEOS and O_3 as in Application Example 2, instead of formation of the second insulating film by means of the plasma CVD method using TEOS and O_2 as in Application Example 3.

Application Example 4

Figure 3 illustrates the steps of formation of an interlayer insulating film for a 2-layer wiring in the manufacturing process of Application Example 4 of this invention. As shown in Figure 3A, circuit elements were formed on Si substrate (2), with first Al wiring (4) (4A-4C) having side surfaces almost perpendicular to the principal surface of the substrate. Then, using the same plasma CVD method as that used in Application Example 1, SiO_2 film (6) with a thickness of 0.6 μm as a first insulating film was deposited on the substrate. Then, as shown in Figure 3B, by means of a dry etching method using Ar and fluorine containing gas in the same way as in Application Example 1, SiO_2 film (6) was etched for 0.3 μm to form SiO_2 film (8) having a slope with angle of 60-85°. Then, as shown in Figure 3C, by means of the same thermal CVD method using a gas mixture of TEOS and O_3 as in Application Example 2, SiO_2 film (9) with a thickness of 0.2 μm was deposited and it covered up the gaps of 0.8 μm or smaller on said Al wiring (4). Then, as shown in Figure 3D, by means of the same plasma CVD method using a gas mixture of TEOS and O_2 as in Application Example 1, SiO_2 film (10) with a thickness of 0.3 μm was deposited. In this case, SiO_2 film (9) prepared using thermal reaction of TEOS has a better step covering property than SiO_2 film (10) prepared using plasma reaction of TEOS, and it is appropriate for covering up gaps of 1 μm or smaller. However, the thermal reaction of TEOS leads to degradation in the film quality of SiO_2 film (9), and cracks may develop in the heat treatment process performed after a thick film is deposited. It is possible to prevent generation of

cracks by depositing SiO_2 film (10) by means of plasma reaction of TEOS. Also, compared with a depositing rate of 0.2 μm/min of SiO_2 film using thermal reaction of TEOS, the depositing rate of SiO_2 film using plasma reaction of TEOS is higher (0.8 μm/min). Consequently, it is possible to increase the throughput. Also, by selecting the thickness of the SiO_2 film using said thermal reaction of TEOS and the thickness of the SiO_2 film using said plasma reaction of TEOS, and by performing said steps of operation repeatedly, it is possible to cover up gaps of said Al wiring (4) with any dimensions.

The same results were obtained when SiO_2 film (6) was etched by means of a dry etching method using O_2 and fluorine containing gas after formation of a resist film in the recessed portions on SiO_2 film (6) as in Application Example 3, instead of etching of SiO_2 film (6) to a slope of 60-85° by means of a dry etching method using Ar and fluorine containing gas as in said Application Example 4.

Effect of the invention

The aforementioned method for manufacturing a semiconductor device in this invention has the following effects. By means of etching a first insulating film with gaps formed on it to form a slope of 60-85° down to the bottom of the gaps and without leaving side surfaces perpendicular to the principal surface of the substrate, it is possible to cover up fine gaps with an aspect ratio of 1 or larger free of voids when a second insulating film is formed.

Because it is possible to cover up fine gaps without generating voids, it is easy to flatten the surface of the semiconductor substrate. When this method is used in forming an interlayer insulating film for a multi-layer wiring, the upper layer of wiring can be formed prepared [sic; easily]. Also, it is possible to prevent wire breakage of the lower layer of wiring. In addition, by realizing multi-layer wiring, the integration degree and operation speed of the elements can be increased.

By means of a combination of the operation of deposition of an insulating film with a pyrolysis reaction of an organic oxysilane and the operation of deposition of an insulating film with a plasma decomposition reaction, it is possible to cover up fine recessions of an insulating film.

As explained above, according to this invention, it is possible to cover up fine recessions of an insulating film without forming voids. Consequently, this invention contributes significantly to an increase in the integration degree and reliability of elements.

Brief description of the figures

Figure 1 presents cross-sectional views illustrating steps in Application Examples 1 and 2 of the method for manufacturing a semiconductor device in this invention. Figure 2 presents

cross-sectional views illustrating steps in Application Example 3 of the manufacturing method of this invention. Figure 3 presents cross-sectional views illustrating steps in Application Example 4 of the manufacturing method of this invention. Figure 4 presents cross-sectional views illustrating steps in an example of a conventional manufacturing method. Figure 5 presents cross-sectional views illustrating steps of another application example of a conventional manufacturing method.

2 Si substrate, 4A, 4B, 4C Al wiring, 6, 8, 9, 10 CVD-SiO_2 film, 7, 7A, 7B, 7C, 7D Resist film.

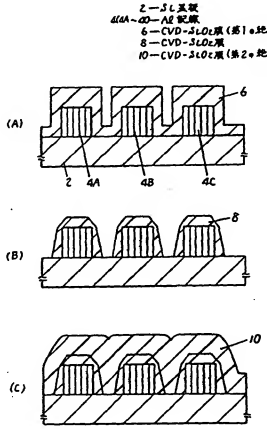

Figure 1

Legend:		
	2	Si substrate
	4 (4A-4C)	Al wiring
	6	CVD-SiO_2 film (first insulating film)
	8	CVD-SiO_2 film
	10	CVD-SiO_2 film (second insulating film)

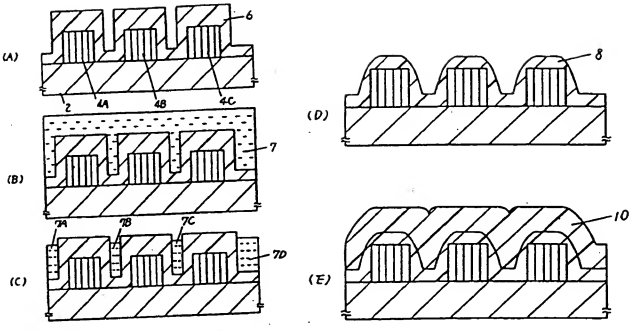

Figure 2

Legend: 7, 7A, 7B, 7C Resist film
8 CVD-SiO_2 film

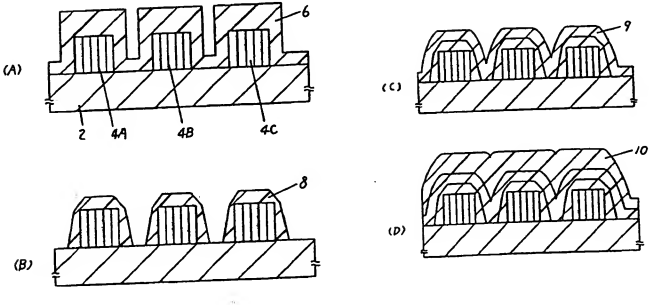

Figure 3

Legend: 9, 10 CVD-SiO_2 film (second insulating film)

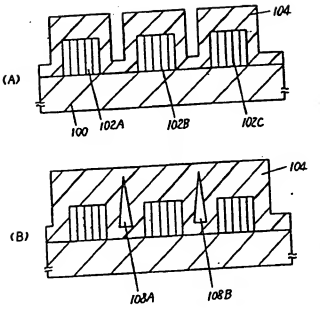

Figure 4

Legend:		
	100	Si substrate
	102 (102A-102C)	Al wiring
	104	CVD-SiO_2 film
	108 (108A, 108B)	Voids

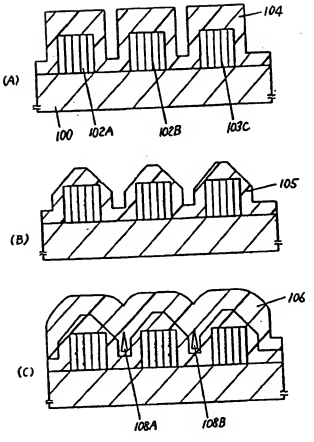

Figure 5

Legend: 105, 106 CVD-SiO_2 film